AN ADAPTIVE DELTA-MODULATION SYSTEM WITH A LOGIC CIRCUIT TO CONTROL STEP SIZE

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ABSTRACT

An experimental adaptive delta-modulation system is described here. Principle of adaptive quantisation is explained. A logic circuit is designed to control step size. The complete delta-modulation system was designed, constructed and tested. Experimentally observed wave forms confirm the variation of the step size in adaptive delta-modulation.

1.0 INTRODUCTION

An important member of the class of differential wave form coders is one-bit or two-level pulse-code modulation (DPCM), better known as Delta-Modulation (DM)[1]. The property of the one-bit codeword eliminates the need for word framing at the transmitter and the receiver, and made DM systems very attractive for many classes of digital communication. The simplicity of DM also makes it an important method for digital voice storage [1].

The simplicity of DM has inspired numerous refinements and variations. At bit rates in the range of 32 to 48 kb/s, DM systems with adaptive quantisers provide reproduction of speech with very good quality, using extremely simple algorithms. The basic principle employed in an adaptive quantiser is to have a quantiser whose step size can be varied from sample to sample according to some suitable algorithm. This variation can be based on the short-term statistics or the long-term variations of the input. Therefore, there are two types of adaptive quantisers, namely the instantaneously adaptive quantiser and the syllabically adaptive quantiser. Ideally, each should be able to adjust its range to changes in the input voltage level so that in each local time epoch, the range would be appropriate for the input signal. Of particular importance are the so-called syllabically adaptive DM systems which have a remarkable degree of robustness to bit error rates in the range of 1%. This property holds good to transmission bit rates as low as 9.6 kb/s and makes DM coders an important means for low bit rate speech digitisation with communications quality [1].

This paper describes an adaptive quantisation delta-modulation (ADM) system with a logic circuit constructed in the laboratory and compares its quantisation-noise performance with an earlier laboratory model of a delta-modulation system [2].

2.0 ADAPTIVE DELTA MODULATION

Figure 1 illustrates the principle of delta-modulation. The difference of an input signal x(t) is quantised to $\pm \Delta$ volts. The resulting quantised signal q(t) is sampled by a clock at a frequency of f_s Hz. The sampled output s(t) is integrated to obtain r(t).

The oversampling ratio F, which is defined as the ratio of the sampling frequency to the Nyquist rate, is typically equal to 1 in multi bit DPCM and much higher in delta-modulation. The transmission bit rate in DM is numerically equal to the sampling rate f_s. Sampling rates of interest in DM span a very wide range, say $100>F>1$. The higher range is used in DM based A/D converters of high precision, whereas DM coders for transmitting waveforms with reasonable quality employ sampling rates of $10>F>1$ [1].

At the receiver, s(t) passes through an integrator (called first order predictor) and a low-pass filter to yield an approximation to the originally transmitted

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input signal x(t) [1, 2, 3, 4, 5, 6].

Rigorous analysis of delta-modulation is extremely difficult, since the comparator (quantiser) has an abrupt discontinuity with a sequence of linear ramp functions of slope Δf_s where Δ is the step size and $T = 1/f_s$ the sampling period. Adaptive delta-modulation (ADM) is a system where the step size is a varying quantity.

If the input signal slope characteristics are not known, wave form encoding in linear delta-modulation (LDM) will be less accurate, with an arbitrarily selected step size being either too small (slope overload) or too large (granularity) [1].

The slope tracking problem is alleviated in adaptive delta-modulation where the step size is allowed to follow variations in the input signal slope. With slowly adaptive or syllabic adaptive coders, the approach is to estimate the average slope of a wave form segment. In instantaneous adaptive coders, the attempt will be to track the instantaneous or local input signal slope by appropriate, albeit abrupt increase or decrease of the step size [1]. **Figure 2** illustrates slope overload distortion and granular noise in linear delta-modulation. Slope mistracking is more obvious in LDM than ADM. A formal quantitative definition of slope overload is difficult and many definitions exist [1].

Granular noise has a variance of $\Delta^2/3$ [1]. The idle channel noise or zero-signal bit pattern ideally consists of alternate ones and zeros: ——— 10 10 10 10 ———.

If the encoding and decoding processes are asymmetrical, the idle channel bit pattern will occasionally have two adjacent ones or zeros say ——— 10 10 11 01 00 11 ———.

ADM systems can also be based on adapting parameters other than step size, for example, adapting output filter bandwidths or sampling rates to follow speech bandwidths, or switching to different sets of predicting pixels in image coding, to follow the changing nature of image. In the literature, ADM almost invariably stands for Delta-Modulation-Adaptive Quantisation (DM-AQ or AQ-DM) [1, 6]. **Figure 3** illustrates an adaptive quantisation delta-modulation system with single integration.

The hybrid constant factor incremental delta-modulation (H.C.F.I.D.M.) can be used for instantaneous as well as syllabic adaptation of the step size Δ. Computer simulation results show that the hybrid schemes are superior to the non-hybrid schemes offering an 8 - 10dB improvement of dynamic range. There is a possibility of improved performance by using microprocessors [7]. The shift register, adaptation logic, adder and multiplier can all be implemented by using a microprocessor (**Figure 4**). The microprocessor can then be programmed to carry out the necessary multiplications, additions and integrations. Because of the high cost of the microprocessor, a hardware implementation was preferred. The block diagram of the ADM is shown in **Figure 5**. The demodulator consisted of the adaptation logic, the integrator and the band-pass filter.

3.0 CIRCUIT DESIGN AND CONSTRUCTION

The design objective had been an ideal coder of large dynamic range, high signal-to-quantisation noise ratio and low cost. It may not be possible to design an ideal coder. The simplicity of the design was the key guiding factor. The system is designed to change the size of the steps by constant factors of 0.5, -0.5, 0, 1, -1 volts.

The input bandpass filter was designed for 300 - 3400 Hz frequency range.

3.1 Adder

The output of the adder is sampled. The logic unit comprising the J-K flip-flop is used as sample and hold circuit.

3.2 Voltage-Controlled Oscillator (VCO)

The VCO provides the clocking pulses for sampling. The IC 741 23, the retriggerable monostable multi-vibrator was connected as a square wave generator whose frequency and duty cycle could be varied [8].

3.3 Shift Register

The shift register acts as the memory corresponding to the four most recent bits. The data bits are serial. The shift register operates in a serial-in parallel-out (SIPO) manner. Data bits are entered by synchronous clock pulses. After four clock pulses, the input word is installed in the register. The clock pulses stop at the moment the data bits are registered and the output bits appear on the output lines.

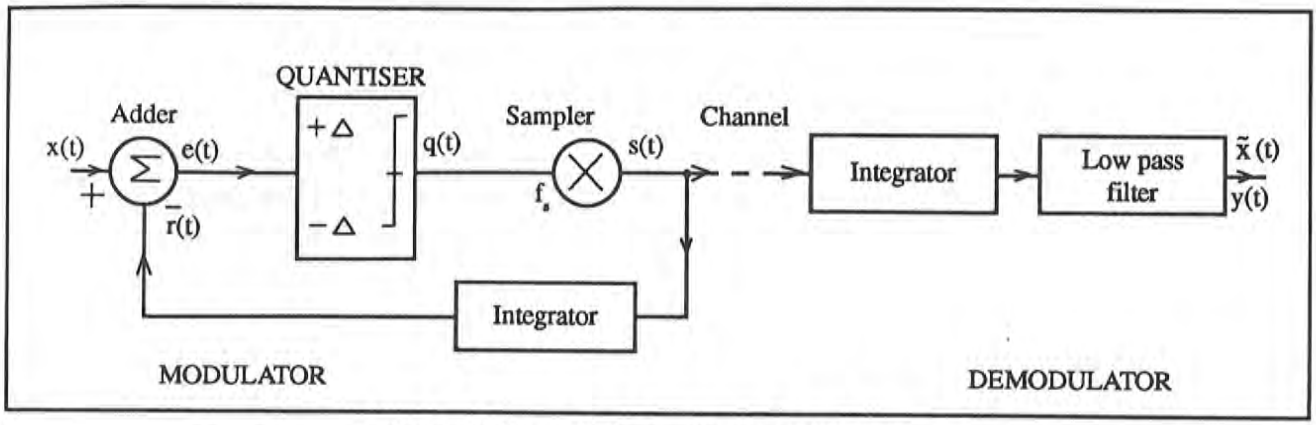

Figure 1: **A Linear Delta-Modulation (LDM) System**

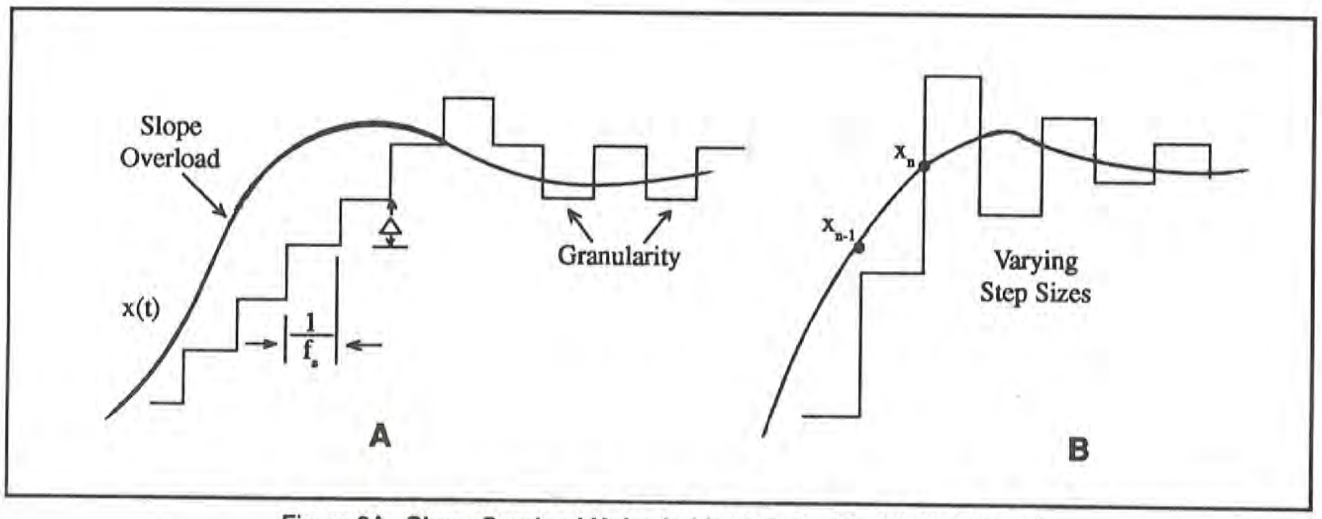

Figure 2A: **Slope-Overload Noise in Linear Delta-Modulation (LDM)**
Figure 2B: **Reduction of Slope-Overload Noise by Varying Step Size in an Adaptive-Delta Modulation (ADM) System**

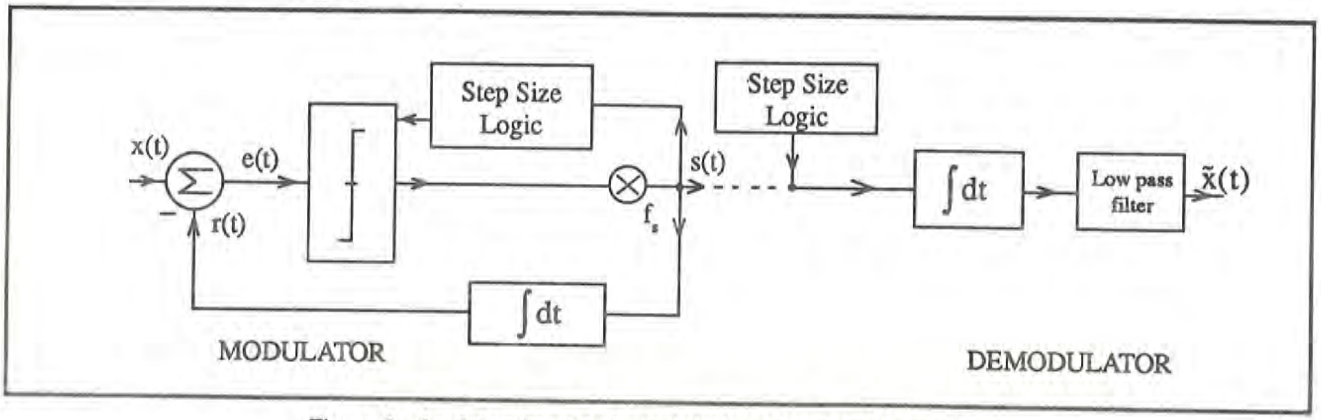

Figure 3: **An Adaptive-Delta Modulation (ADM) System with a Logic Circuit to control Step Size**

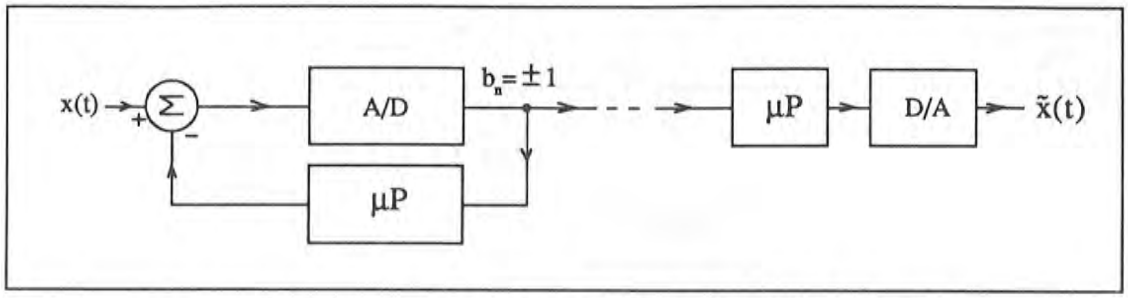

Figure 4: **A Microprocessor controlled Delta-Modulation System**

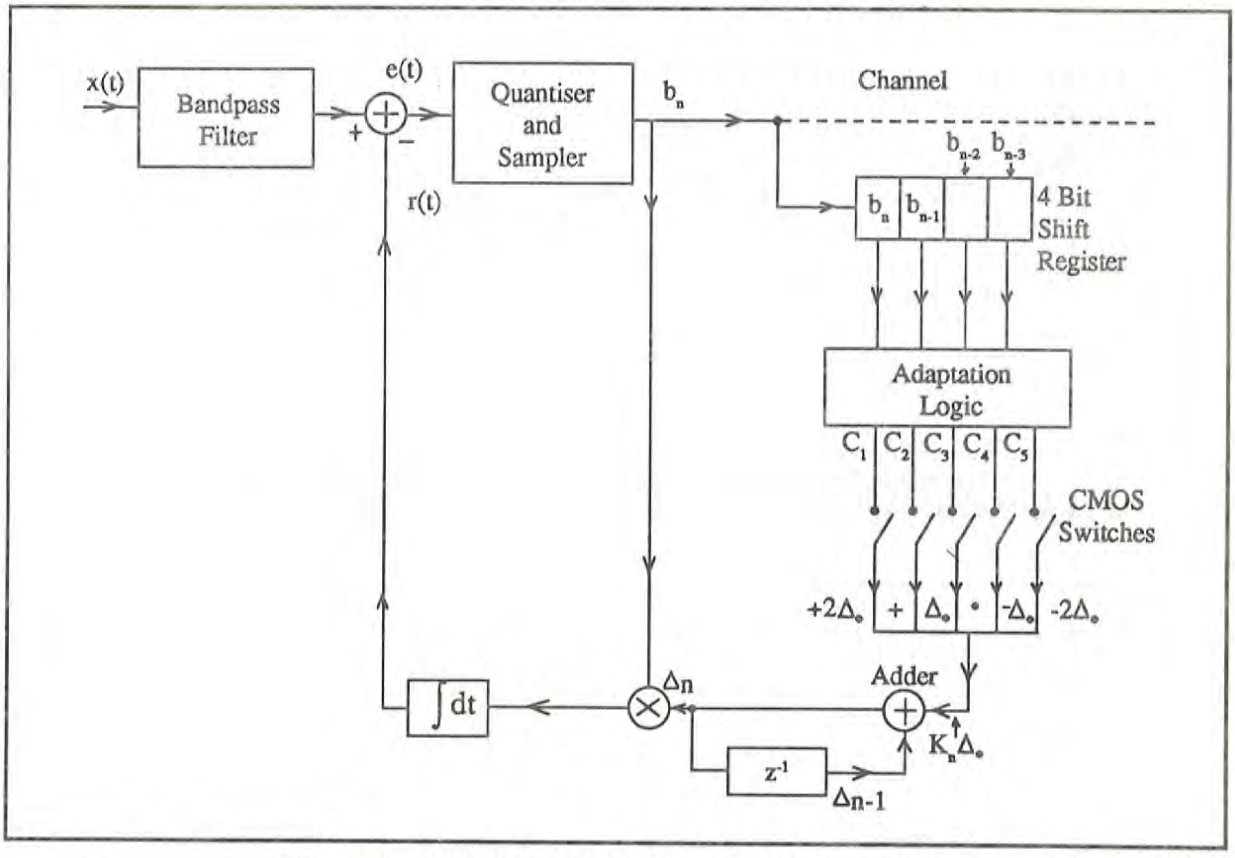

Figure 5: **Implementation of Adaptive-Delta Modulator with a Logic Circuit to control Step Size**

To ensure that four data bits are latched to the logic unit, a parallel-in, parallel-out (PIPO) shift register is connected to a SIPO register. The clock to the PIPO is four times slower than that of the SIPO. A binary counter acts as a clock to the PIPO.

3.4 Adaptive Logic Circuit

The adaptation logic unit detects slope overload and the threshold levels. The logic unit receives its input from the PIPO output. The logic unit checks for the 16 possible combinations of 4 input bits. The logic unit output is high for only one of the possible 16 combinations. The switching speed of the gates is of the order of few nanoseconds. Adjacent alternating ones and zeros (1100) or four alternating ones and zeros (1010) indicate slope overload.

The adaptation logic unit is the intelligence to control the step size. By studying all sixteen combinations, a scheme was devised to change the step size (increase or decrease) by a constant factor of two to one. Using the Karnaugh map, the logic output equations are as follows:

$$C_1 = \overline{A}\overline{B}\overline{C} + ABC$$

$$C_2 = AB\overline{C}D + \overline{A}\overline{B}C\overline{D}$$

$$C_3 = \overline{C}\overline{D}B + CD\overline{B}$$

$$C_4 = \overline{A}B\overline{C}D + A\overline{B}\overline{C}D + \overline{A}BC\overline{D} + A\overline{B}C\overline{D}$$

$$C_5 = \overline{A}BCD + A\overline{B}\overline{C}\overline{D}$$

The adaptation logic circuit diagram is shown in Figure 6.

3.5 CMOS Switches

The adaptation logic circuit outputs C1, C2, C3, C4, C5 are connected to five CMOS Switches. The CMOS switch was chosen because of its high speed of operation. Whenever a logic high appears at the logic circuit output, the CMOS switch is turned on. Only one switch turns on at any instant.

3.6 Time Delay Unit

A time delay is required to hold Δ_{n-1} and this was achieved by using two LF 398IC's and a 555 timer IC. The arrangement consisted of two sample and hold circuits with different clock periods.

3.7 Summing Operation

The outputs of the five CMOS switches are applied as five inputs to a unity-gain summing amplifier. The IC5534 was used as the operational amplifier. The summing amplifier performs the following operation (Figure 5).

$$|\Delta_n| = |\Delta_{n-1}| + K_n\Delta_o$$

By summing the five outputs, a staircase wave form is obtained. The amplitudes of the staircase wave form (constant factors K_n) gives the amount by which the bits b_n must be changed. The change of the step size were $\pm 1, \pm 0.5, 0$ volt.

3.8 Integrator, Lowpass and Band-Pass Filter

The integrator reconstructs the input signal from the delta-modulator output. The integrator network consists of an op-amp with resistor and capacitor.

Instead of a low-pass filter at the demodulator, a band-pass filter is employed to eliminate high frequency noise. An active fourth-order Butterworth bandpass is implemented with 3dB cutoff frequencies at 300 and 3,400Hz. It is realised by cascading a second-order low-pass section with a second-order high-pass section. The associated Butterworth polynomial is $(s^2 + 0.765\,s + 1)\,(s^2 + 1.848\,s + 1)$.

4.0 SYSTEM PERFORMANCE AND DISCUSSION

Based on the block diagram of Figure 5, the circuits for the various blocks were designed. The complete circuit diagram is quite complicated and is not given here. The complete system was constructed in the laboratory on breadboards.

Figure 7 displays the results of wave form measurements made on the adaptive delta-modulation system. Figure 7A shows the sinusoidal input wave form x(t) applied to the modulator and the demodulator output $y(t) = \overline{x}(t)$. These wave forms correspond to the situation when the switches are exactly in the same position on the modulator and the demodulator sections. When the switches at the modulator and the demodulator are not exactly in the same position, then there is an error of transmission and this error is shown

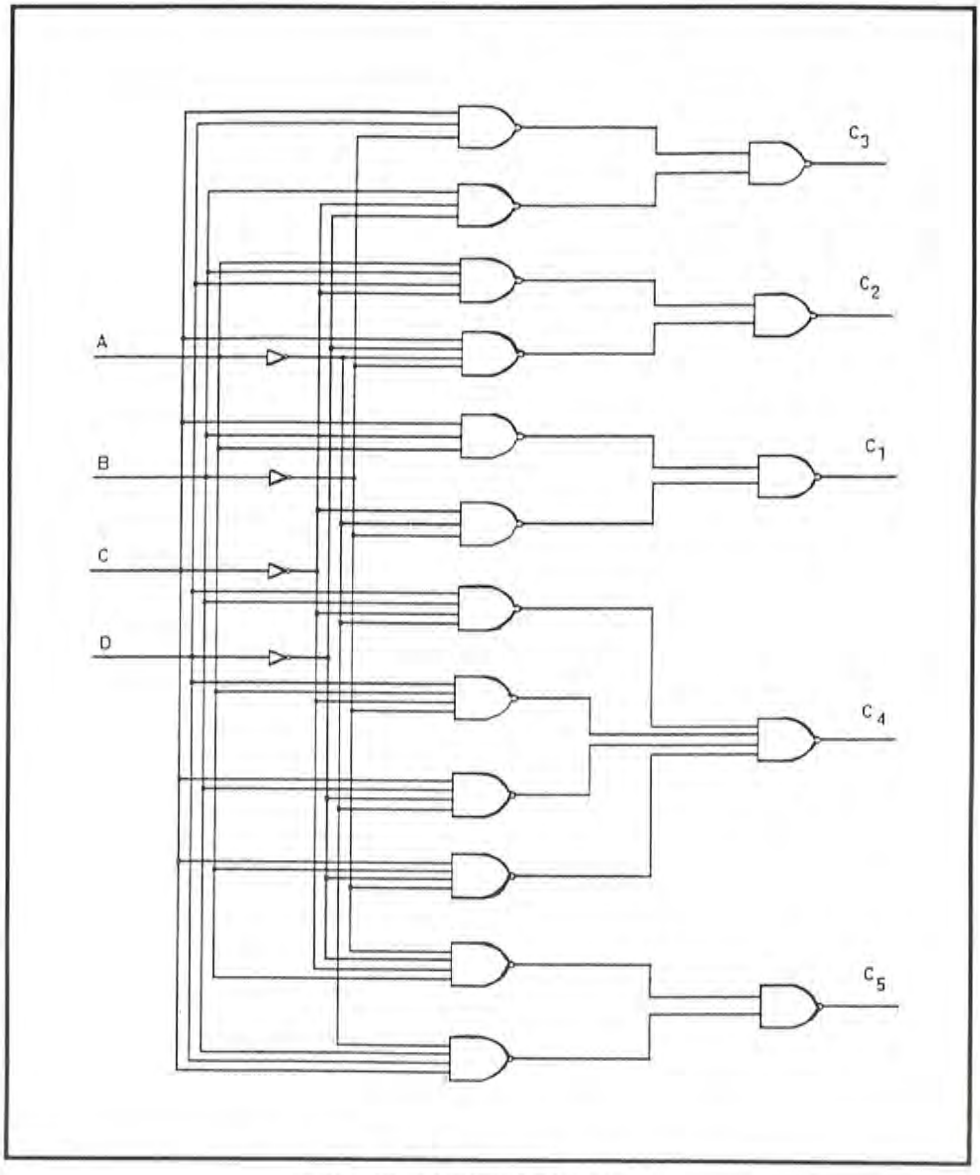

Figure 6: **Adaptive Logic Circuit**

in **Figure 7B**. The transmission error wave form represents the different step sizes at the modulator (upper wave form) and the demodulator (lower wave form).

A significant factor determining the delta-modulation performance is the step size Δ. If it is too large or too small, system performance is not optimum and the approximated signal does not match the input signal x(t).

The step functions of the present adaptive delta-modulation system are shown in **Figure 7C** and **7D**. The step function at the demodulator is the wave form shown in the **Figure 7C** and the step function of the modulator is the wave form shown in **Figure 7D**. It indicates the appropriate amount of change in the step size at the modulator. The spikes in the wave forms are due to circuit noise. Circuit noise is generated due to a number of contacts at the power supply line.

Thus, experimentally obtained results correspond to the theoretical expectations. The change in the step

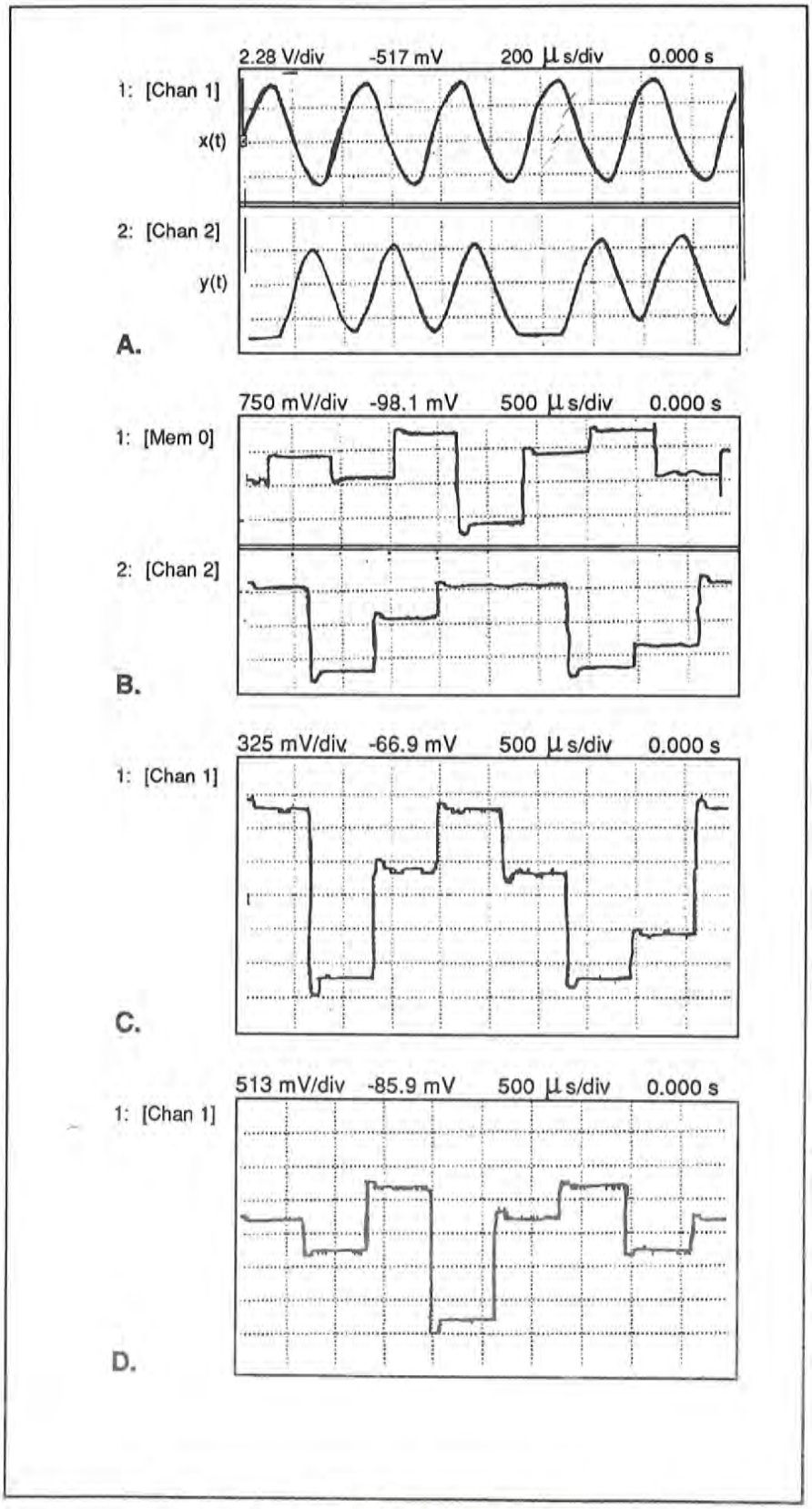

Figure 7: **Adaptive Delta-Modulation Waveforms**

size as given by the expression

$$|\Delta_n| = |\Delta_{n-1}| + K_n \Delta_o$$

is experimentally observed and verified. The results of Figure 7 confirm this expression.

It was observed that the quantisation noise performance of this ADM system at a sampling frequency of 17kHz was identical with that of the previously constructed linear DM system at a sampling frequency of 52kHz.

5.0 CONCLUSION

The aim of building a working model of an adaptive delta-modulation system was achieved. The step size changed by the constant voltage levels of half volt and one volt. The step size changes instantaneously. The adaptation logic circuit operation is very fast, being of the order of a few nano-seconds. The logic circuit is capable of handling sixteen different combinations of most recent four bit data and thus it reduces slope overload noise.

The overall system performance can be enhanced by combining the hardware with software. By using the software, an optimum and satisfactory algorithm can be derived to obtain the reconstructed version of the sample output.

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